

Circuit design technique for high efficiency Class F amplifiers

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In this paper, lead network circuit technique to design high efficiency Class F amplifiers using new types of loading circuits was demonstrated. The loading circuits were realized using both lumped elements and transmission lines. The derived values of each circuit element are given. The simulation procedure and experimental verification were performed on the example of high-voltage LDMOSFET power amplifier. The test measurements show that, for this power amplifier, 76% drain efficiency can be achieved for 20 W output power at 500 MHz operating frequency.

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